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(71) Applicant: eMagin Corporation [US/US]; 2070 Route 52, Hopewell Junction, NY 12533 (US).

(72) Inventors: PRACHE, Oliver, F.; 213 Manville Road, Pleasantville, NY 10570 (US). HONGJIN, Eric, Kim; 3 Preston Court, Bedford, MA 01730 (US). SASHI, D., Malaviya; 5 Orbit Lane, Hopewell Junction, NY 12533 (US). HAIQUNG, Lin; 6850 Sanctuary Court, Elkridge, MD 21075 (US). NAVAISKY, Eric; 844 Governors Run, Ellicott City, MD 21043 (US). EBNER, John; 1900 Thames Street #332, Baltimore, MD 21231 (US).

(74) Agent: PERRY, Guy; Skadden, Arps, Slate, Meagher & Flom LLP, Four Times Square, New York, NY 10036 (US).

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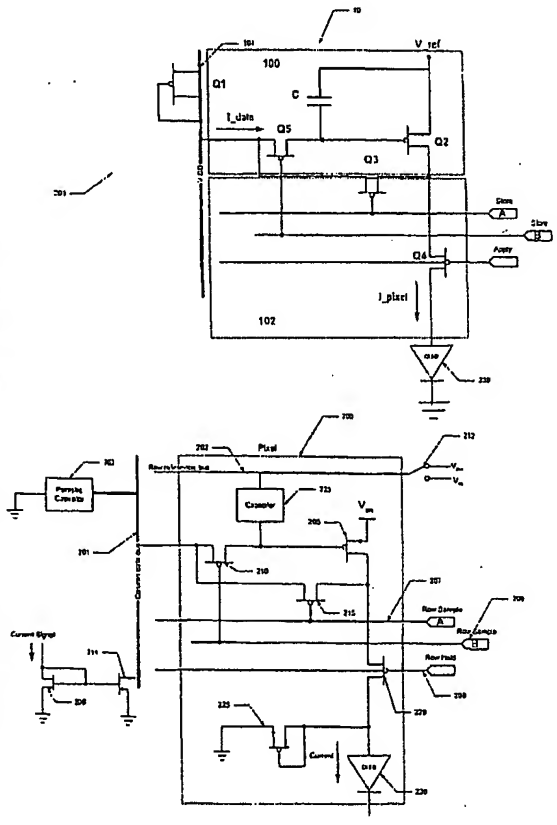
(54) Title: A CURRENT-TYPE DRIVER FOR ORGANIC LIGHT EMITTING DIODE DISPLAYS



(57) Abstract: An OLED Driver circuit decreases capacitance charging time in the driver circuit by providing a high current signal to the circuit during a sample phase which rapidly charges the capacitances. A lower current signal is then provided during a hold phase to drive the corresponding OLED. The current levels are produced by operating the current driver of the circuit in the sub-threshold region where the output current is exponentially proportional to a reference voltage. The reference voltage may be controlled to provide a difference in reference voltage that produces the desired output current reduction. The driver circuit also includes a voltage driver that pre-charges the current driver gate to reduce settling time. The pre-charge level is provided during an initial portion of a sample phase to reduce the time it takes for the voltage at a current driver gate of the circuit to reach the desired signal level. The pre-set voltage is either selected by reference to the input signal level or by reference to a global level. In one implementation the global level is the black-level voltage for the corresponding display.

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TITLE OF THE INVENTION

A CURRENT-TYPE DRIVER FOR ORGANIC LIGHT EMITTING DIODE DISPLAYS

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority to a provisional application filed July 18, 2000, serial number 60/218,798, entitled "CURRENT PIXEL FOR HIGH SPEED DISPLAY DEVICE."

BACKGROUND OF THE INVENTION

The invention relates to electrical circuits for driving individual elements of an electronic display, and more particularly to controlling the current supplied to an Organic Light Emitting Diode ("OLED") in an OLED display.

OLEDs, which have been known for approximately two decades, are desirable for use in portable micro displays because they combine high levels of luminance and color with small pixel sizes and low power consumption. Future "near-to-the-eye" microdisplay applications, such as portable DVD viewers and digital cameras, would require OLED pixel sizes of less than 100 square micrometers, with pixel current dynamic ranges of from a few hundred picoamperes to tens of nanoamperes. Such microdisplays would further require good matching between the OLED pixels to maintain uniformity in the display. Furthermore, it would be advantageous to use less expensive process technologies, such as digital CMOS, to mass-produce such microdisplays in a cost-effective manner.

However, it is not possible to meet these requirements for OLED microdisplays using known methods of driving OLEDs in matrix addressed graphics displays. It is well known that the luminance of an OLED is proportional to the amount of current applied to the OLED. There are two known methods used to

modulate the current delivered to an OLED from a current source.

A first known method employs a voltage driver to directly modulate the gate voltage of a current source transistor by a voltage signal. A second method employs a current driver to convert video signals to current signals and uses conventional CMOS current mirrors to copy the current signals into the OLED driver.

The voltage driver approach has a number of shortcomings. The drain-source current of a MOSFET transistor operating in linear mode is exponentially proportional to the gate-source voltage. Thus, in order to modulate the current applied to an OLED by the requisite small amount, an even smaller range of voltages must be applied to the gate of a MOSFET acting as the current source. In addition to the general difficulty of generating such low voltage levels, the presence of any ambient noise in the circuit substantially interferes with low-level signals, making this method impractical for microdisplays.

The current driven approach is also hampered by major disadvantages. One drawback is related to settling time. The level of current applied to the OLED pixel is extremely low – only a few hundred picoamperes at the first gray level. But the chip size of an OLED microdisplay is comparatively large – almost the size of a stamp when millions of pixels are grouped together. The direct transfer of low-level current across a large chip requires a long time because of the need to charge all the parasitic capacitors. A long settling time makes it impractical to achieve the video bandwidth required in microdisplay applications.

SUMMARY OF THE INVENTION

The present invention is an improved OLED pixel driver circuit comprising a MOS transistor acting as a current source that operates in the sub-threshold region, where the current is exponentially proportional to the gate-source voltage. The pixel

driver circuit has a sample phase and a hold phase. In one embodiment, during a sample phase, a large-scale programming current is sampled at the driving current source. During a hold phase, a fixed voltage step is applied to the gate of the current source, which scales down the programming current by a predetermined fixed factor. The scaled down current is used to drive the OLED pixel.

In another embodiment, in order to improve settling time, the OLED pixel driver employs a high bandwidth voltage driver to charge the gate of the current source prior to, or at the start of, the sample phase. The voltage pre-set scheme greatly improves settling time in the driving circuit of the present invention, which allows for greater video bandwidth. The voltage pre-set scheme is preferably used with the improved OLED pixel driver described above, but may also be employed with other current-type drivers.

In another embodiment, the invention provides a sample and hold pixel current driver circuit for supplying current to an OLED. The circuit includes a first transistor that is coupled to a data bus for providing input current signals during a sample phase of the circuit. The circuit also includes a second transistor having a source which may be coupled to a current supply, a drain, and a gate for regulating the flow of current from said source to said drain. The circuit further includes a sample switching circuit including a first switch, which has a first control for opening and closing the first switch. The sample switching circuit also includes a second switch, which has a second control for opening and closing the second switch. The sample switching circuit includes a capacitor, which has two electrodes. The first switch has an input coupled to the data bus and an output coupled to the first capacitor electrode and to the gate of the second transistor. The first capacitor electrode is coupled to the gate of the second transistor while the second electrode is coupled to a voltage reference.

Finally, the second switch is coupled between the data bus and the drain of the second transistor. The circuit also includes a hold switch having an input coupled to the drain of the second transistor, a hold switch control for opening and closing said hold switch, and an output which may be coupled to an OLED.

In yet another embodiment, the invention provides a method for supplying current to an OLED in an OLED display. The method provides a first transistor on a data bus of the display. The first transistor has a channel width to length (W/L) ratio, whereby the current flow from the first transistor is proportional to the W/L ratio. The method couples the data bus to a second transistor and to a capacitor during a store phase to store a data level by providing a first current to the capacitor. The second transistor also has a W/L ratio, whereby the current flow from the second transistor is proportional to the W/L ratio. The method then decouples the data bus from the second transistor and from the capacitor. Finally, the method couples the second transistor to an OLED to provide a second current from the transistor to the OLED during an apply phase, whereby the second current is proportional to the second transistor W/L ratio and to the data level stored in the capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a diagram illustrating the physical structure of an OLED;

Figure 1B is a schematic diagram illustrating the general structure of a driver circuit of the invention;

Figure 2A is a schematic diagram illustrating an OLED pixel driver store and apply circuit in accordance with the invention;

Figure 2B is a timing diagram for the signals in the circuit of Figure 2A;

Figure 3 is a schematic diagram illustrating an OLED driver circuit in accordance with the invention;

Figure 4A is a graph illustrating the general transconductance characteristic of a MOSFET;

Figure 4B is a timing diagram for signals in the circuit of Figure 3;

Figure 5 is a schematic diagram of an OLED pixel driver circuit with a voltage level pre-set, derived from an input signal;

Figure 6 is a schematic diagram of an OLED pixel driver circuit with a voltage level pre-set tied to a global reference voltage;

Figure 7 is a timing diagram for signals in the circuit of Figure 6; and

Figure 8 is a schematic diagram of an OLED driver circuit equivalent to the circuit of Figure 6 during the sample phase.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1A is a diagram illustrating the physical structure of an OLED of the invention. An OLED generally includes a light-emitting layer of a luminescent organic solid and adjacent semiconductor layers that are sandwiched between a cathode and an anode. The cathode and the anode serve as electrodes to conduct current through the organic layer. The current causes electrons to flow to holes in the doped organic materials and thereby produce light.

In the example of Figure 1A, a first layer of silicon oxide **21** is provided on the silicon wafer **20**. An electrode material for an anode **22** is then formed on the silicon oxide layer **21**. An organic layer is provided on the anode **22**. The organic layer of the illustrated OLED includes a hole injection layer **24**, a hole transport layer **26**, an electron transport layer **28**, and an electron injection layer **30**. A cathode **32** is formed over the organic layer. A moisture barrier layer **33** is formed over the cathode **32**. Finally, a color conversion layer **34**, which improves luminance and electrical connectivity, is formed over the moisture barrier layer **33**.

In operation, when a potential difference is applied across the device, negatively charged electrons move from the cathode to the electron-injecting layer and finally into the layer of organic material. At the same time, positive charges, typically referred to as holes, move from the anode to the hole-injecting layer and into the organic material. When the positive and negative charges meet in the organic material, photons are produced.

In a matrix-addressed OLED graphics display, individual OLEDs are formed on a single substrate and arranged in a grid pattern. Several OLEDs, forming a column of the grid, preferably share a common cathode line. Several OLEDs, forming a row of the grid, preferably share a common anode line. Individual OLEDs emit light when their cathode line and anode line are simultaneously activated. In some configurations, a group of OLEDs within the matrix forms one pixel in a display, with each OLED usually serving as one sub-pixel, or pixel cell.

The conventional method of transporting a driving signal to a pixel is to use a voltage signal provided from a data line to control the application of driving current to the light-emitting portion of the pixel. Thus, a typical pixel may include a current source selectively connected to the light emitting material through a MOS transistor. The gate of the transistor is connected to the voltage source and tied to a capacitor so that the transistor can store the voltage used to control the image produced by the LED. The current source is employed to power the light-emitting element because these elements typically emit an amount of light that is linearly proportional to the MOS transistor current. The current output of a MOS transistor, however, is highly (nearly exponentially) sensitive to the gate voltage of the transistor. Accordingly, as the current required to achieve particular levels of gray scale decreases, the voltage stored on the capacitor tied to the gate electrode decreases even more rapidly. This

relationship makes it increasingly difficult to generate the correct voltage required for the precise gray scale control. Furthermore, as a result of the high sensitivity of control to the gate voltage, small errors in voltage from interference noise, process variation, or aging may produce severe spatial and/or temporal non-uniformity in luminance. It is therefore extremely difficult to control gray scale in microdisplays using a voltage source.

The sensitivity of the luminance controlling transistor to gate voltage variation may be addressed by using a current source to control the transistor gate. If a current is used to control the gate of the transistor used to apply current to the LED, however, then the activation speed of the pixel may become an issue. Low activation speeds may make the LED unsuitable for many, if not all, applications.

In order to address need for high activation speeds, it has been determined that the highly capacitive data line used to supply current to the transistor gate may be driven at a current level considerably higher than needed for LED emission. Consequently, only a portion of the current on the data line needs to be sampled into the pixel to activate the transistor gate. This partial sampling of the current may be accomplished by making use of a circuit similar to that of a current mirror. This circuit may include a pair of two MOS transistors of the different size. The larger transistor may be located on the data line and the smaller transistor may be located in the pixel. This arrangement may result in only a part of the current on the data line being mirrored into the pixel. As a result, current may be used to control the application of a driving current to the LED without making significant speed concessions.

In accordance with the foregoing, high speed and high fidelity displays may be produced. High speed may be achieved by designing a pixel that allows the highly

capacitive data line to be driven with a very high current level. High fidelity may be achieved by controlling the current used to drive the pixel with relatively noise-immune current instead of noise-susceptible voltage.

Figure 1B is a schematic diagram of a driver circuit in accordance with the invention, which provides such advantages. The circuit **10** is preferably used to provide current to an OLED **230**. The circuit includes a means for storing and applying a driving current **100**, a switch **102**, and a data line **104**. The circuit **10** is useful for driving pixels using an analog signal from the data line **104** such that all pixels have the same light emitting period while being provided different gray shades in accordance with signal magnitude.

The data line **104** selectively provides a control signal in the form of a current to the means for storing and applying a driving current **100**. In one embodiment, the data line **104** is connected to a plurality of OLEDs (pixels). The current from the data line **104** is preferably significantly greater than the current required to operate the OLED **230** in order to facilitate high speed response to signals provided on the data line **104**. The switch **102** is used to periodically and selectively connect the data line **104** to the means for storing and applying a driving current **100**. The means for storing and applying a driving current **100** is in a storage mode when it is coupled to the data line **104**. During an applying mode, the means for storing and applying a driving current **100** is preferably adapted to provide the pixel with a reduced current level, as compared to the current level during the storage mode.

With reference to Figure 2A, a detailed schematic diagram of an embodiment of the invention is shown. The means for storing and applying a driving current **100** of Figure 1B is instituted by a portion of the circuit **10** including a driving transistor **Q2**, a store transistor **Q5**, and a capacitor **C**. The current switch **102** of Figure 1B is

instituted by a portion of the circuit 10 including a row transistor **Q3** and a switching transistor **Q4**. In one embodiment, each of the foregoing transistors is implemented as a MOSFET transistor. A data line transistor **Q1** is preferably provided on the data line **104**. The data line transistor **Q1** and the data line **104** may be shared by a plurality of circuits.

With reference to the operation of the circuit **10** and Figure 2B, when the corresponding pixel (i.e., OLED **230**) is selected, the voltages at the gates of the row transistor **Q3** and the store transistor **Q5** are set to a low level (time **A**), and the circuit **230** is placed into the storing mode. During the time interval **A-B**, the data line transistor **Q1** and the driving transistor **Q2** are connected to each other through the row transistor **Q3** and the store transistor **Q5** to form a current-mirror-like pair. As a result of the connection of the data line transistor **Q1** with the driving transistor **Q2**, the capacitor **C** stores a charge to turn on **Q2**. As shown in Figure 2B, the transistor **Q4** is used to switch off the pixel current during the charging of the capacitor **C**.

The Width to Length ratio (W/L ratio) of the channel in the data line transistor **Q1** is selected to be large as compared with the W/L ratio of the driving transistor **Q2** so that the pixel current (I_pixel) is small as compared with the storage current (I_data). In one embodiment, the level of I_data is selected based upon the desired response speed of the pixel to pixel information sent on the data line **104**. In order to increase response speed, I_data is increased. In another embodiment, the level of I_pixel may be selected based upon the desired response speed of the pixel to pixel information sent on the data line **104**. In order to increase response speed, I_pixel is decreased. In yet another embodiment, the level of I_pixel may be selected based upon the desired emission intensity of the diode **230**. In order to increase emission intensity, I_pixel is increased. Thus, the determination of the desired current levels

for I_data and I_pixel dictates the sizes of the transistors **Q1, Q2**, since the current ratio of I_pixel to I_data is determined by the ratio of the sizes of the transistors **Q2, Q1**. It is appreciated that for a typical high-speed display, the current ratio of I_data to I_pixel may vary widely depending upon the desired intensity of the diode **230** and other factors such as required response speed.

If the required current ratio (I_data to I-pixel) is too large to be handled by adjusting the W/L ratios of the transistors **Q2, Q1**, alone, the gate-to-source voltage of **Q2** can be reduced in magnitude by a fixed amount after the storage capacitor has been charged up by the data line **104**. This can be accomplished by changing the reference voltage on a reference bus, as discussed below.

When the pixel is not selected, the gate voltages at the row transistor **Q3** and the store transistor **Q5** go high (time B as shown in Fig. 2B), **Q4** is on and current flows through the diode **230**. During the applying mode, the diode **230** is caused to luminesce due to the application of the voltage stored on the capacitor **C** through the driving transistor **Q2**.

Figure 3 is a schematic diagram of an OLED pixel driver circuit in accordance with the invention. The pixel driver circuit **200** includes a current source **205**, a pair of sample switches **210, 215**, a hold switch **220**, a clamp **225**, an OLED **230**, and a capacitor **235**. In one embodiment, the current source **205**, the pair of sample switches **210, 215**, the hold switch **220**, and the clamp **225** are transistors. In this embodiment, the transistors are preferably MOSFET devices. Each MOSFET device preferably includes a source, a gate, and a drain, as is known in the art. The current source of this embodiment is preferably a PMOS device.

The current source **205** preferably operates in sub-threshold region, as discussed below. The capacitor **235** preferably functions as a memory device, storing

the pixel data during each video frame. A parasitic capacitor **202** is also illustrated as an example of capacitance effects that are associated with the driving circuit **200**.

A column data bus **201** is preferably used to carry data signals for a column of pixels in the OLED display. The column data bus **201** is coupled to the exemplary parasitic capacitor **202**, to a data current source **206**, and to the source inputs of the sample switches **210, 215**. A column data transistor **214** provides the data current signal from the data current source **206** to the column data bus **201**.

A row reference bus **203** is coupled to a toggle switch **212**, which selects between a high voltage (V_{BH}) and a low voltage (V_{BL}) for the row reference bus. In one embodiment, the toggle switch **212** is controlled by a display control unit (not shown). The row reference bus **203** is also coupled to a first electrode of the capacitor **235**.

Row sample control lines **207, 208** are coupled to the gate inputs of the sample switches **210, 215**. The drain of the first sample switch **210** is coupled to a second electrode of the capacitor **235** and to the gate of the current source **205**. The drain of the second sample switch **215** is coupled to the drain of the current source **205** and to the source of the hold switch **220**. The source of the current source **205** is preferably coupled to a voltage source (V_{an}). A row hold control line **209** is coupled to the gate of the hold switch **220**. The drain of the hold switch **220** is coupled to the anode of the OLED **230**. The drain of the hold switch **220** is also coupled to the clamp **225**. In one embodiment, the clamp **225** functions as a protective diode, which prevents the voltage at the anode of the OLED **230** from falling below a predetermined minimum voltage level.

In operation, the OLED driver circuit **200** can be viewed as a sample-and-hold circuit, having a sample phase and a hold phase. Preferably, the driver circuit **200**

stores pixel data during the sample phase, while providing the stored data to the corresponding OLED during the hold phase. Figure 3B illustrates signal levels on the first row sample control line **207**, the second row sample control line **208**, the row hold control line **209**, and the row reference bus **203**.

Referring now to Figures 3 and 4B, during the sample phase, the sample switches **215, 210** are turned on by the signal levels on the first row sample control line **207** and on the second row sample control line **208**, respectively. The hold switch **220** is turned off by the signal level on the row hold control line **209**. Also during the sample phase, the row reference bus **203** is coupled to the lower reference voltage, V_{BL}, by the toggle switch **212** moving to the corresponding voltage input. Since the sample switches **210, 215**, are on, the gate and drain of the current source **205** are shorted together, operatively coupling the current source **205** to the column data bus **201**. Column data is provided on the column data bus **201**. The column data current flows through the sample switches **210, 215**, and charges the capacitor **235**. The column data current also flows to charge the parasitic capacitor **202**. When one pixel is in the sample phase, all the other pixel drivers on the same data line are preferably in the hold phase so that only the target pixel samples the column data from the data bus. After the parasitic capacitor **202** and the capacitor **235** are charged to the desired level in accordance with the column data, the circuit is ready to supply current to the associated OLED during the hold phase.

In the hold phase, the first sample switch **210** and the second sample switch **215** are turned off by the corresponding signals on the first row sample control line **207** and the second row sample control line **208**. Notice in Figure 4B that the first sample switch **210** is turned off earlier than the second sample switch **215** to isolate capacitor **235** so that the input data is set only by capacitor **235**. The hold switch **220**

is turned on by the signal on the row hold control line 209. The current source gate 205 is thereby disconnected from the column data bus 201 and the current source drain is switched to the OLED anode. The toggle switch 212 moves from the lower voltage, V_{BL}, to the higher reference voltage, V_{BH}, raising the voltage at the capacitor first electrode by $(V_{BH} - V_{BL})$. Accordingly, the voltage at the capacitor 235 second electrode, and the current source 205 gate, is also raised by $(V_{BH} - V_{BL})$. The increase in voltage V_{GS} at the gate of the current source 205 results in a scaling down of current, I_{DS}, which is provided by the driver current source 205, because the current source is operating in the sub-threshold region (Figure 3). In one embodiment, such scaling is set to provide a two orders of magnitude (1/100) reduction in the output current of the pixel driver. As may be appreciated, as long as the value of the step $(V_{BH} - V_{BL})$ is constant, the actual values of V_{BH} and V_{BL} are not significant. Thus, the OLED is driven by a current from the capacitor 235, which is within the small driving current range that is required by the OLED. In other embodiments, where an NMOS current sink is used instead of the PMOS current sink (current source 205), the voltage during the first phase is lower than the voltage during the second phase.

Figure 4A is a graph illustrating the general transconductance characteristic of a MOSFET. Referring to Figures 3 and 4A, when the gate-source voltage of the current source 205 is greater than the current source intrinsic state voltage and less than the current source threshold voltage (V_T), the current source operates in the sub-threshold region. In this region of operation, the drain-source current ("I_{DS}") is exponentially proportional to the gate-source voltage ("V_{GS}"). Thus, a small change in V_{GS} causes a much larger change in I_{DS}. Accordingly, during the sample phase, the lower reference voltage at the current source gate results in a high current flow I_{DS} through the current source 205. As may be appreciated, when the reference voltage is

increased during the hold phase substantially lower current flows through the current source **205**. The sample phase current is preferably much larger than the pixel data current, for example, by 100 times. Thus, the capacitor **202** and the parasitic capacitors on the data bus **201** are charged at a fast rate, which decreases settling time.

In another embodiment, shown in Figure 5, a driver circuit **200** includes a voltage driver **245**, which is used to pre-charge the current driver gate. Since the input data signal on the column data bus **201** is a low current signal, the sample phase is often slew limited, i.e., the time period of the sample phase is limited by the time it takes the voltage at the current driver gate to reach the desired level. The operation of the driver circuit of Figure 5 includes a pre-set phase, in addition to the sample phase and the hold phase. During the pre-set phase, the gate of the current source **205** is pre-charged so as to decrease its settling time. Referring now to Figure 5, a voltage driver **245** (shown as an OP-AMP) has an output selectively coupled to the column data bus **201** by a switch **214**. The voltage driver **245** has a feedback input coupled to the voltage driver output and a reference input coupled to the gate and drain of a reference current driver **224**. The voltage driver reference input is also coupled to the drain of a reference transistor **228**. The reference transistor **228** has a drain coupled to ground level and a gate coupled to a data current signal source **206**.

By employing a voltage driver **245** on the column data bus, the current source gate is pre-charged during the sample phase, decreasing the settling time of the current source **205**. Figure 7 illustrates signals on the first row sample control line **207**, the second row sample control line **208**, the hold control line **209**, and the output of the pre-set switch **214**. As may be appreciated from Figure 7, the pre-set phase is initiated prior to or at the start of the sample phase to speed up the settling of the current source **205**. In operation, during the pre-set phase, the sample switches are

turned on by the corresponding signals on the first row sample control line **207** and the second row sample control line **208**. Accordingly, the signal from the column data bus **201** is applied to the gate of the current source **205**. The pre-set switch **214** provides the pre-set level to the gate of the current source **205** by way of the column data bus **201**. Preferably, after the pre-charge level is reached, the voltage driver **245** is disconnected by opening the pre-set switch **214**, allowing the level at the current source gate to settle according to the input signal current on the column data bus **201**. During hold phase the circuit operates substantially the same as the circuit of Figure 2, as discussed above. As may be appreciated, the pre-charging of the current source gate during the programming phase also reduces the time for charging the parasitic capacitor **202**.

Settling time is heavily impacted by the selected pre-set voltage level. In Figure 5 the voltage level pre-set is derived from the input signal. Accordingly, the pre-set voltage charges the pixel driver as close to the desired final level as possible. However, at times, due to cost and production constraints, it may be difficult to refer to the input data signal to select the pre-set level because of the requirement for a determination on a per-pixel basis. Accordingly, in another embodiment, illustrated in Figure 6, the driver uses a constant level global voltage reference to provide pre-set voltage to the current source **205** during the programming phase. Preferably, the reference voltage is selected so as to set the initial current to a level that is lower than the input signal current in the sample phase. Accordingly, the reference voltage is selected, in one embodiment, as the black level voltage, which produces the black level current which represents the smallest signal that would be provided by **206**.

The pre-set phase, as well as the configuration of Figures 5 and 6, can be implemented with various driving circuit configurations to reduce settling time for a

current source. In Figure 6, the circuit includes the row reference bus **203** of Figure 3, in addition to the pre-set voltage driver **245**. Accordingly, as may be appreciated, the pre-set phase is applicable to a variety of voltage controlled current driver circuits.

Figure 8 is a schematic diagram of an equivalent OLED driver circuit during a sample phase in the circuit of Figure 6. The description below, in combination with Figure 8, illustrates why the settling time is shorter when the initial current in the current source **205** is set lower than the programming current, as opposed to higher than the programming current.

Referring to Figure 6, during the sample phase, the sample switches **210** and **215** are turned on and the hold switch **220** is turned off. The current source **205** is connected as a diode and is switched to the data bus, while the OLED **230** is disconnected. Accordingly, Figure 8 illustrates the driver circuit **200** under this state. To analyze the current settling of the current source **205**, let:

I(0) = the initial source-to-drain current of the current source **205**;

I1 = the programming current;

I(t) = the source-to-drain current of the current source **205**.

Because of the large gate capacitance of the current source **205**, including the holding capacitor **235** and the parasitic capacitance **202** on the data bus, it is practical to assume that V(t), the gate voltage of current source **205**, is slew limited. As is known, the slew rate is provided by:

$$\frac{dV}{dt} = \frac{I(t) - I_1}{C} \qquad (1)$$

Let T = programming time (i.e., the time interval between the end of the pre-set phase and the end of the sample phase). From (1), we have:

$$T = \int_{V(0)}^{V(T)} \frac{dt}{dV} dV = \int_{V(0)}^{V(T)} \frac{C}{I(t) - I_1} dV \qquad (2)$$

Since the size of the current source transistor **205** is limited by the pixel size in the OLED display, the current source **205** operates in the sub-threshold mode, for most practical cases. Assume that the source-to-drain voltage of the current source **205** is $V_{SD} > \frac{3kT}{q} = \frac{1}{\beta}$. Therefore, the source-to-drain current of the current source **205** is exponentially proportional to the source-to-gate voltage $V_{sg} = V_{an} - V$. The currents can be written as:

$$I(t) = Is \cdot e^{\beta(V_{an} - V(t))} \quad (3)$$

$$I(0) = Is \cdot e^{\beta(V_{an} - V(0))} \quad (4)$$

$$I_1 = Is \cdot e^{\beta(V_{an} - V_1)} \quad (5)$$

where V_1 is the gate potential of current source **205** when its source-to-drain current equals I_1. Substituting (3) and (5) into (2), we get:

$$T = \frac{C}{I_1}\left[V(0) - V(T) + \frac{1}{\beta}\ln\frac{e^{\beta V_{SG1}} - e^{\beta V_{SG(0)}}}{e^{\beta V_{SG1}} - e^{\beta V_{SG(T)}}}\right] \quad (6)$$

Letting:

$$\Delta I(0) = I_1 - I(0) = Is(e^{\beta V_{SG1}} - e^{\beta V_{SG(0)}}) \quad (7)$$

$$\Delta I(T) = I_1 - I(T) = Is(e^{\beta V_{SG1}} - e^{\beta V_{SG(T)}}) \quad (8)$$

equation (6) becomes:

$$T = \frac{C}{I_1}\left[V(0) - V(T) + \frac{1}{\beta}\ln\frac{\Delta I(0)}{\Delta I(T)}\right] \quad (9)$$

Given equation (9) and realizing that $e^{\beta(V(T) - V(0))} = \frac{e^{\beta \cdot V(T)}}{e^{\beta \cdot V(0)}} = \frac{e^{\beta(V_{an} - V(0)}}{e^{\beta(V_{an} - V(T)}} = \frac{I(0)}{I(T)}$, we have:

$$\Delta I(T) = \frac{I_1 \cdot \Delta I(0)}{\Delta I(0) + I(0) \cdot e^{\beta(\frac{I_1}{C}T)}} \cong \frac{\Delta I(0) \cdot I_1}{I(0) \cdot e^{\beta(\frac{I_1}{C}T)}} \quad (10)$$

Thus, although it may seem that setting I(0) much smaller that I_1 will slow down the settling, equation (10) actually indicates that it is desirable to choose I(0) to be the black level current, because the term $e^{\beta(\frac{I_1}{C}T)}$ in the denominator increases exponentially with I_1. Therefore, it is at low current levels that the circuit needs more boost. By setting I(0) at or close to, the minimum current level, the term $\frac{\Delta I(0)}{I(0)} = \frac{I_1}{I(0)} - 1$ will reach, or be close to, zero when the signal I_1 is at or close to the black level current, thus reducing settling time.

Accordingly, in order to optimize settling time, the pre-set voltage reference is set to prove the initial current at the current source **205** as equal to or lower than (to compensate offset) the black signal level current.

Although the present invention was discussed in terms of certain preferred embodiments, the invention is not limited to such embodiments. A person of ordinary skill in the art will appreciate that numerous variations and combinations of the features set forth above can be utilized without departing from the present invention as set forth in the claims. Thus, the scope of the invention should not be limited by the preceding description but should be ascertained by reference to claims that follow.

CLAIMS

1. A sample and hold pixel current driver circuit for supplying current to an OLED, said circuit comprising:

a first transistor coupled to a data bus for providing input current signals, the first transistor providing input current signals during a sample phase of the circuit;

a second transistor having a source which may be coupled to a current supply, a drain, and a gate for regulating the flow of current from said source to said drain;

a sample switching circuit including a first switch having a first control for opening and closing said first switch, a second switch having a second control for opening and closing said second switch, and a capacitor having first and second electrodes, said first switch having an input coupled to said data bus and an output coupled to said first electrode and said gate of said second transistor, said first electrode being coupled to said gate of said second transistor and said second electrode being coupled to a voltage reference, and said second switch being coupled between said data bus and said drain of said second transistor; and

a hold switch having an input coupled to said drain of said second transistor, a hold switch control for opening and closing said hold switch, and an output which may be coupled to an OLED.

2. A method for supplying current to an OLED in an OLED display, comprising:

Providing a first transistor on a data bus of the display, the first transistor having a channel width to length (W/L) ratio, the current flow from the first transistor being proportional to the W/L ratio;

coupling the data bus to a second transistor and to a capacitor during a sample phase to store a data level by providing a first current to the capacitor, the second transistor having a W/L ratio, the current flow from the second transistor being proportional to the W/L ratio;

decoupling the data bus from the second transistor and from the capacitor;

coupling the second transistor to an OLED to provide a second current from the transistor to the OLED, the second current being proportional to the second transistor W/L ratio and to the data level stored in the capacitor.

3. The method of Claim 2, wherein the ratio of the first current to the second current is directly related to the ratio of the W/L ratio of the first transistor and the W/L ratio of the second transistor.

4. The method of Claim 2, wherein the response speed of the OLED display is increased by increasing the first current.

5. The method of Claim 2, wherein the emission intensity of the OLED display is increased by increasing the second current.

6. A circuit for driving a light emitting diode in a display using current supply, the circuit comprising:

A driving transistor having a source, drain, and gate, the driving transistor being adapted to selectively provide a driving current to the light emitting diode;

means for providing a data signal in the circuit, the data signal comprising a current greater than the current required to operate the light emitting diode; and

means for diverting a portion of the data signal current to the driving transistor to selectively cause the driving current to be applied to the light emitting diode.

7. A pixel current driver circuit for supplying current to an OLED, said circuit comprising:

a current source having an input which may be coupled to a current supply, a current output, and a control input for regulating the flow of current from said input to said output;

a reference bus having a switch for connecting said reference bus to a first voltage level during a sample phase and to a second voltage level during a hold phase;

a data bus for providing input current signals;

a sample switching circuit including a first switch having a first control for opening and closing said first switch, a second switch having a second control for opening and closing said second switch, and a capacitor having first and second electrodes, said first switch having an input coupled to said data bus and an output coupled to said first electrode and said control input of said current source, said first electrode being coupled to said control input and said second electrode being coupled to said reference bus, and said second switch being coupled between said data bus and said output of said current source; and

a hold switch having an input coupled to said output of said current source, a hold switch control for opening and closing said hold switch, and an output which may be coupled to an OLED.

8. The driver circuit of Claim 7, wherein the first voltage level on the reference bus is lower than the second voltage level on the reference bus.

9. The driver circuit of Claim 7, wherein the first voltage level on the reference bus is higher than the second voltage level on the reference bus.

10. A method for controlling a current source in a current driver circuit of a pixel in an OLED display, the current source having a gate, a source, and a drain, the method comprising:

providing a first signal to the gate of the current source, the first signal corresponding to a data input signal;

providing a reference signal to the gate of the current source, the voltage level at the gate of the current source from the first signal and the reference signal being lower than a threshold voltage level of the current source;

directing the output current from the current source to a memory element to store a signal level;

reducing the voltage level provided by the reference signal;

providing the stored signal level from the memory element to the gate of the current source; and

directing the output current from the current source to an anode of a corresponding OLED.

11. A display apparatus, comprising:

a plurality of pixel elements arranged in a matrix, each pixel element associated with a column and a row;

a plurality of voltage controlled pixel drivers, each pixel driver associated with a pixel element, each pixel driver providing current to an associated pixel element by reference to a data signal on a data input of the pixel driver, each pixel driver associated with a column and a row;

a plurality of column data lines, each column data line providing the data signals to the pixel drivers associated with the column;

a plurality of row control lines, each row control line selectively activating one or more rows of pixel drivers;

a voltage pre-set source selectively coupled to each column data line, the voltage pre-set, during the updating of each row, providing current to the column data line that is derived from at least a level associated with the black level of the pixels.

12. A method for providing data signals to voltage controlled sample and hold pixel drivers in a display having row control lines and column data lines while reducing the settling time of current source transistors, comprising:

providing a row sample signal on the row control line to transition a row of the display to the sample phase;

providing data signals on the column data lines;

coupling a pre-set current source to the column data lines, the pre-set current being provided by reference to the resultant voltage level at the current

source transistor gate when the current source transistor gate settles to a level associated with a minimum luminance data signal;

decoupling the pre-set current source from the column data line prior to the end of the sample phase; and

providing a row hold signal on the row control line to transition the row to the hold phase and provide the sampled data to the associated pixels.

13. A pixel driver in a display apparatus, the display apparatus having a data input bus and reference bus means having one of two voltage levels, comprising:

current supplying means, said current supplying means controlled by a reference voltage level at a control input, said control input operatively coupled to said reference bus means, said current supplying means further including an output;

memory means for storing data from the data input bus; and

selective coupling means, said selective coupling means selectively coupling the memory means to the data input bus and selectively coupling the output of said current supplying means either to said memory module or to an associated pixel element.

14. A pixel current driver circuit for supplying current to an OLED, said driver circuit comprising:

a current signal source for supplying signals;

a current driver circuit having switches for operating in a sample phase mode and a hold phase mode, and a capacitor, for receiving said signals during said sample phase mode for charging said capacitor, and for providing an output

current during said hold mode, which output current being a function of said signal input, for operating an OLED; and

an auxiliary power source selectively coupled to said capacitor during at least part of said sample phase mode for shortening the charge time of said capacitor.

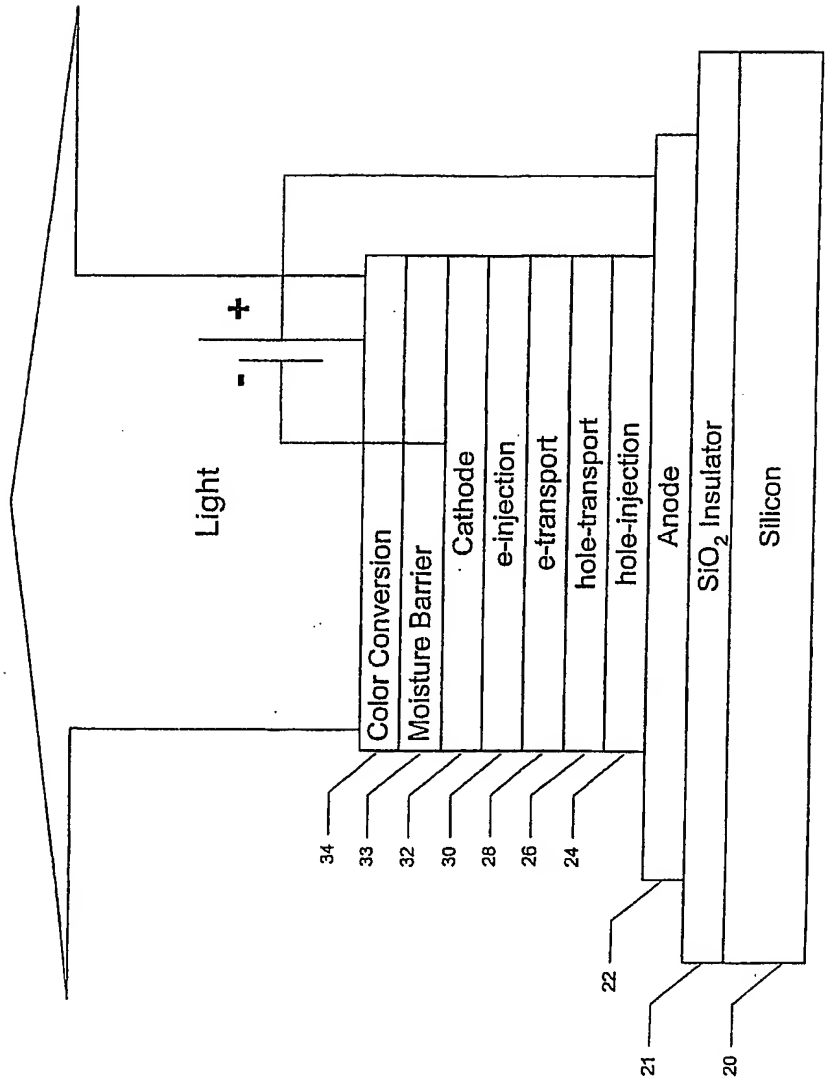
Light
+
-
Color Conversion
Moisture Barrier
Cathode
e-injection
e-transport
hole-transport
hole-injection
Anode
SiO_2 Insulator
Silicon
34
33
32
30
28
26
24
22
21
20

Figure 1A

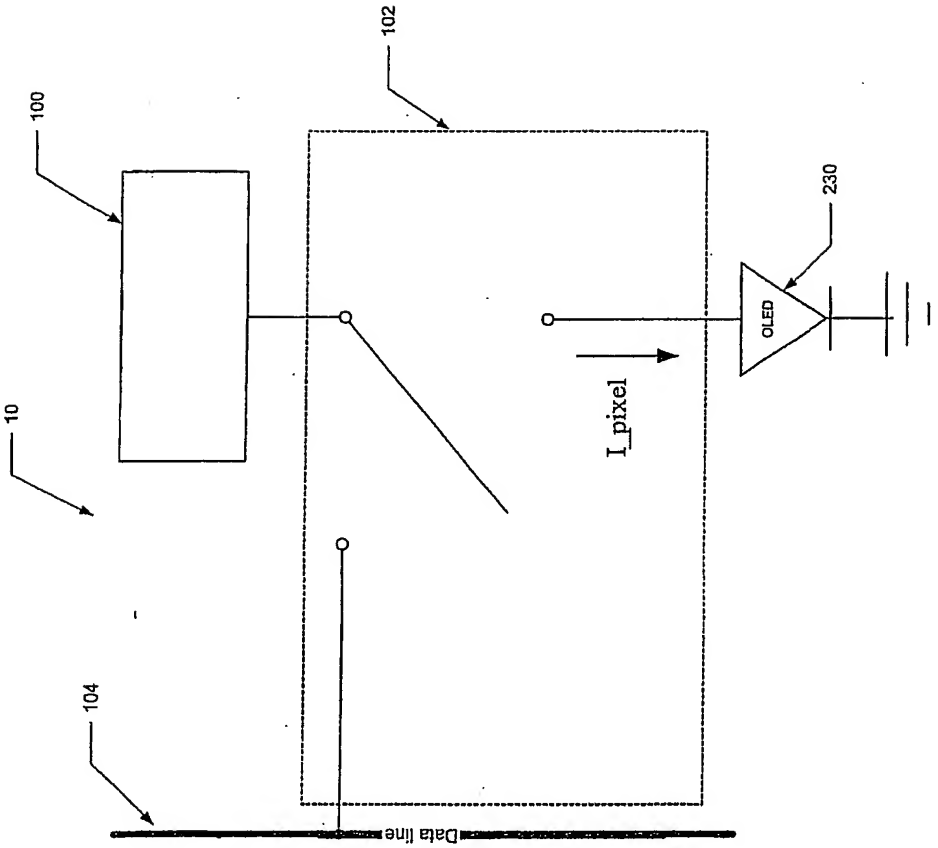

Figure 1B

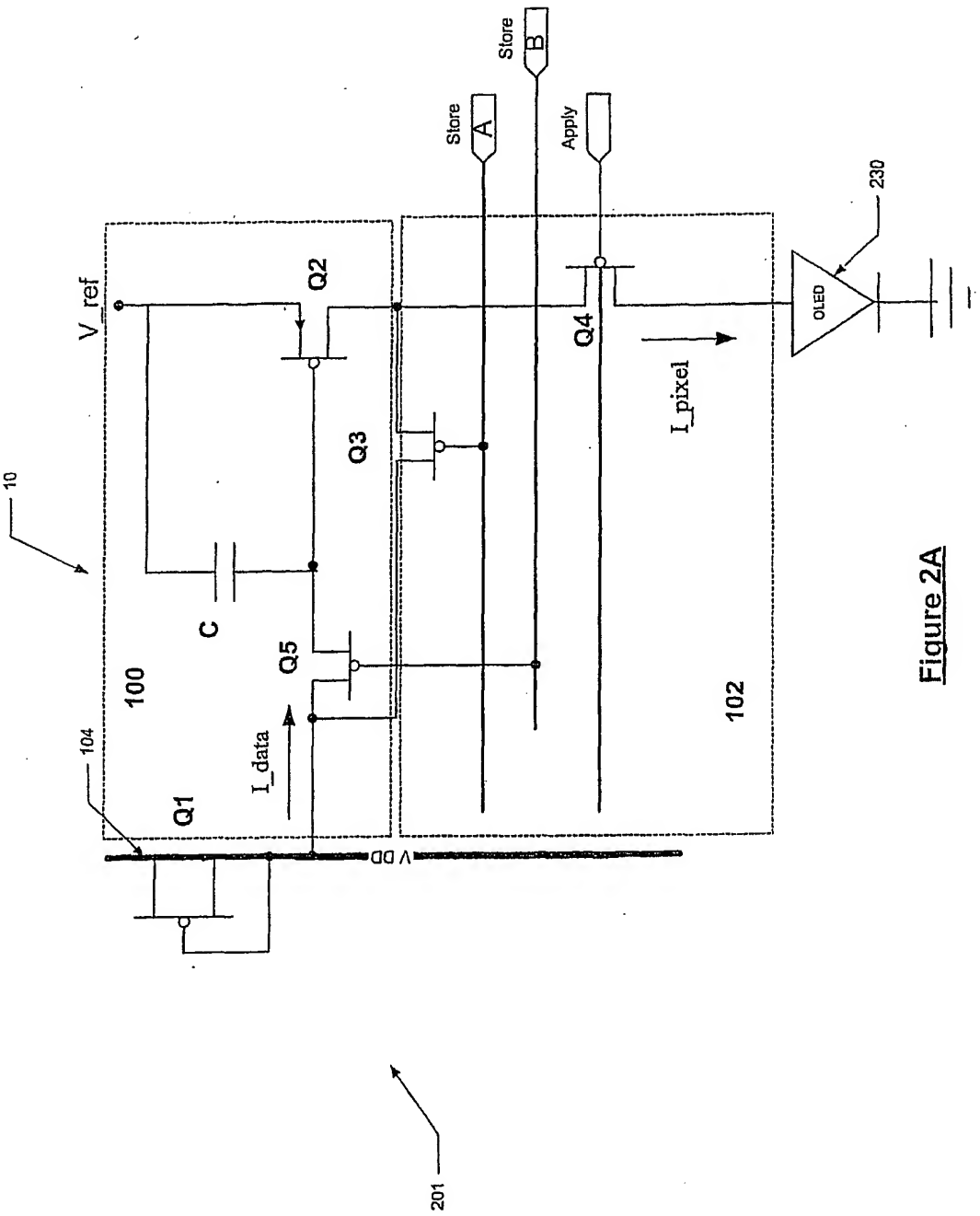
Store
B
Store
A
Apply
230
OLED
V_ref
Q2
Q4
Q3
I_pixel
10
C
Q5
100
102
104
I_data
Q1
V DD
201

Figure 2A

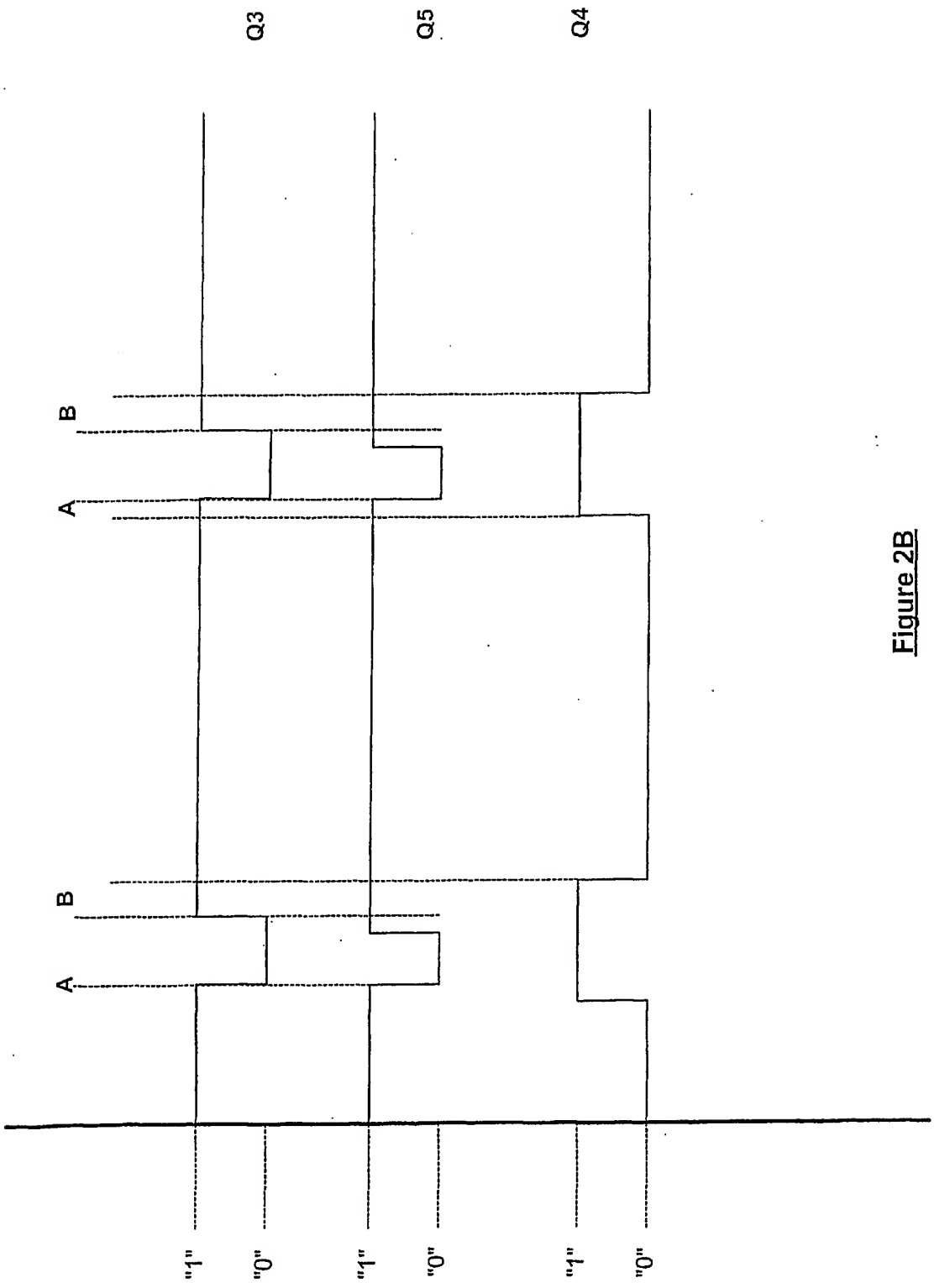

Figure 2B

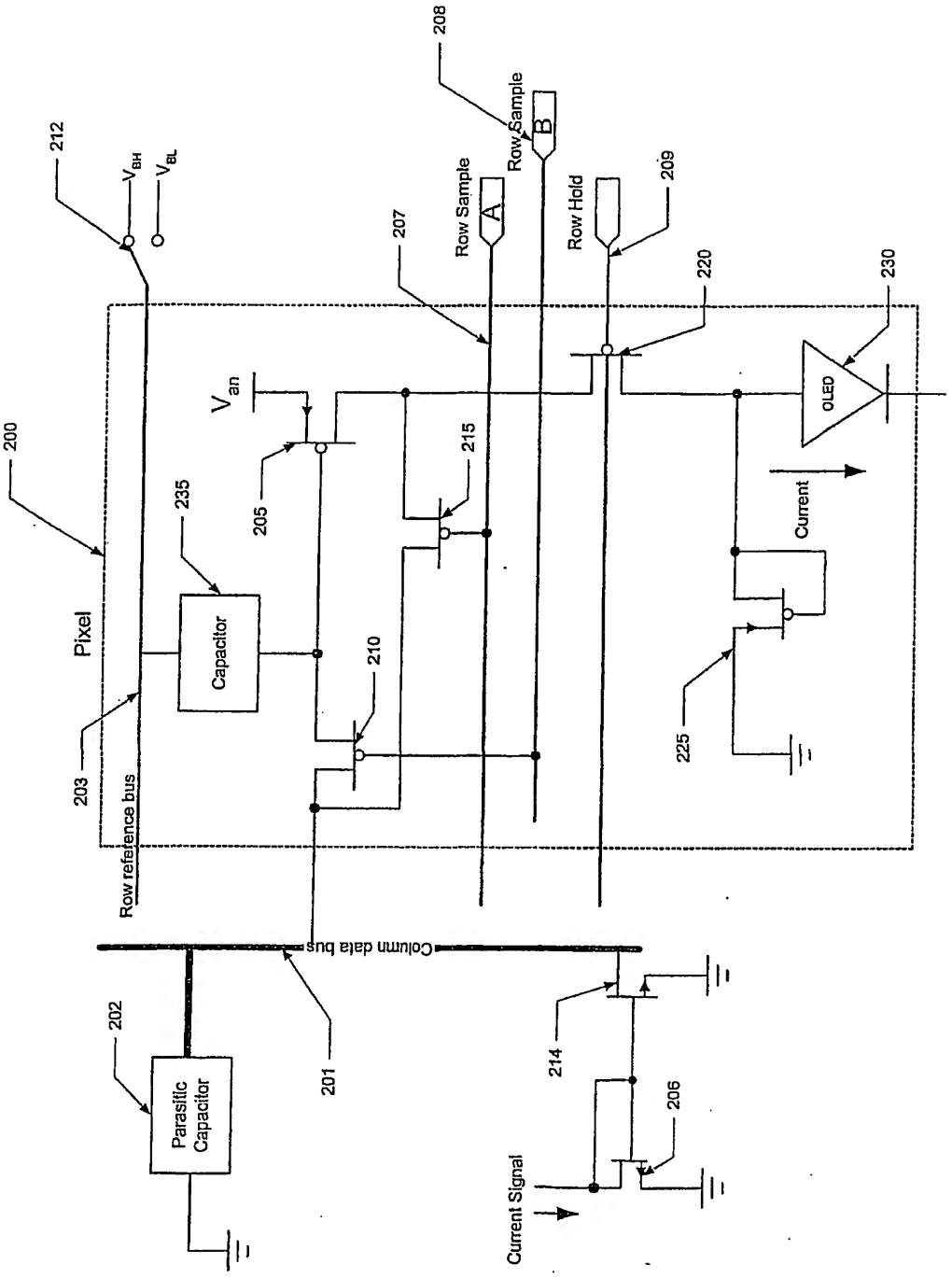
208
Row Sample
B
212
V_{BH}
V_{BL}
Row Sample
A
Row Hold
209
207
220
230
OLED
V_{an}
200
205
215
Current
235
Capacitor
Pixel
210
225
203
Row refefence bus
Column data bus
202
201
214
Parasitic Capacitor
206
Current Signal

Figure 3

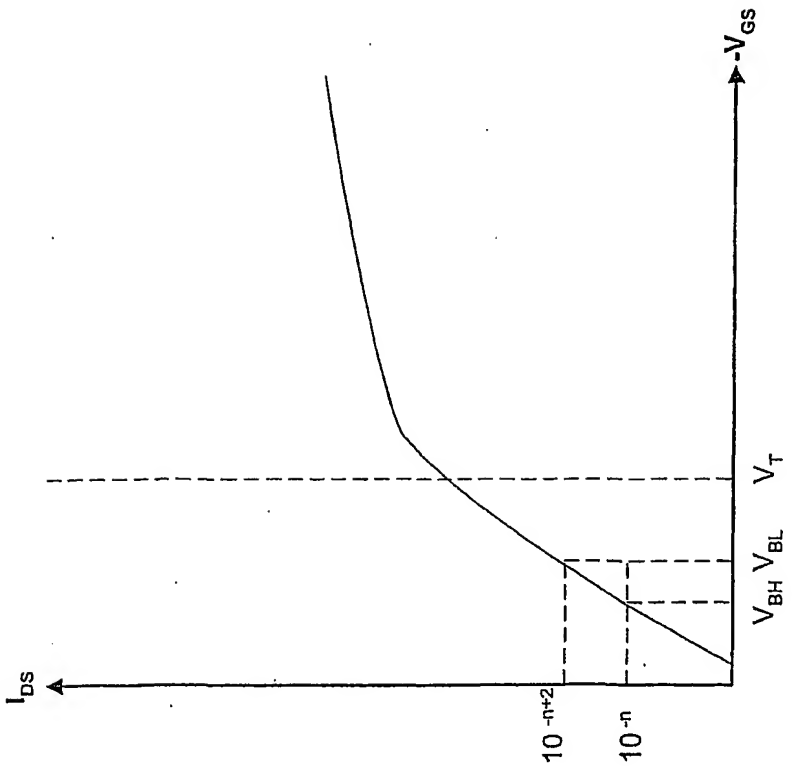

Figure 4A

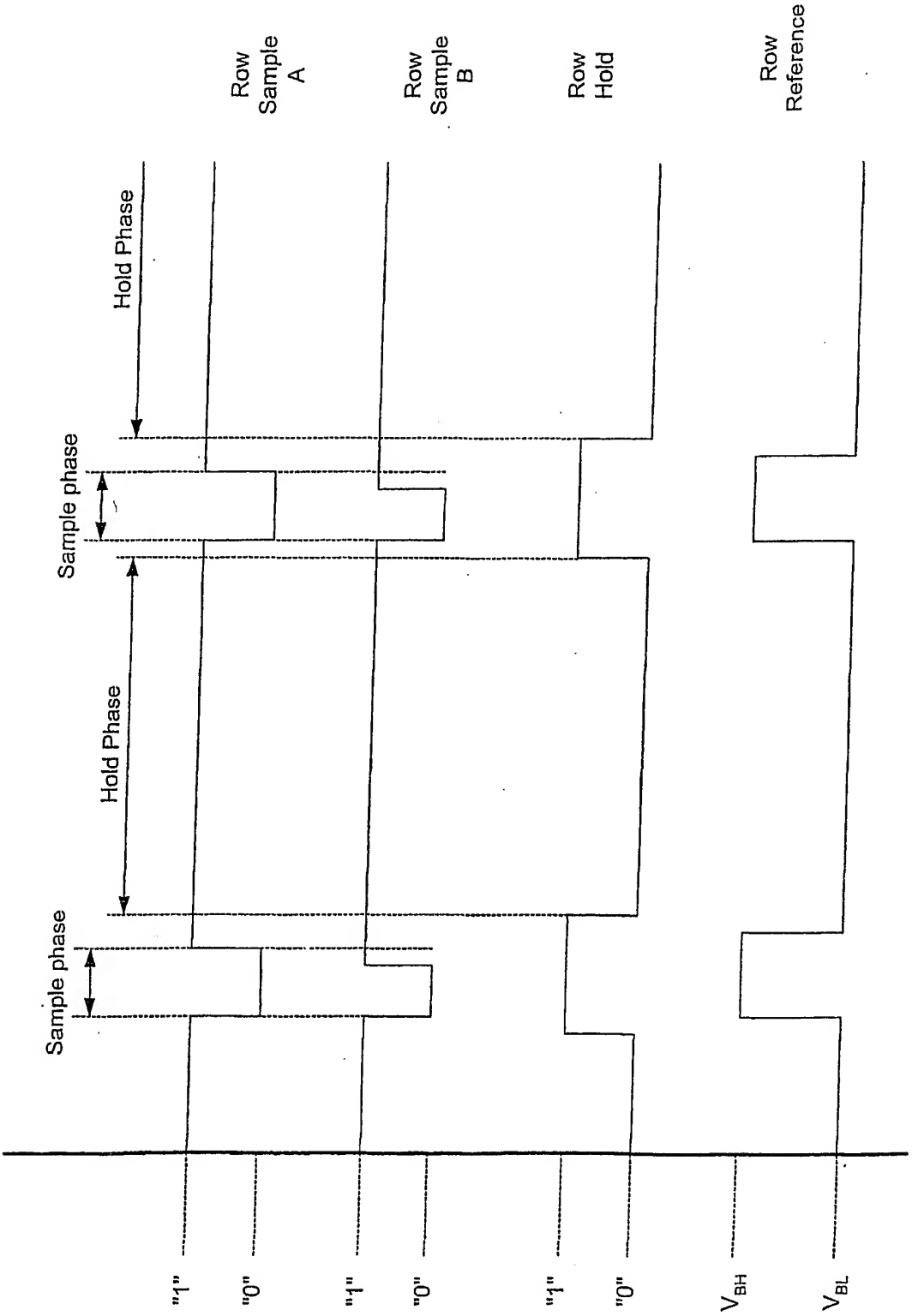
Row Sample A
Row Sample B
Row Hold
Row Reference
Hold Phase
Sample phase
Hold Phase
Sample phase
"1"
"0"
"1"
"0"
"1"
"0"
V_{BH}
V_{BL}

Figure 4B

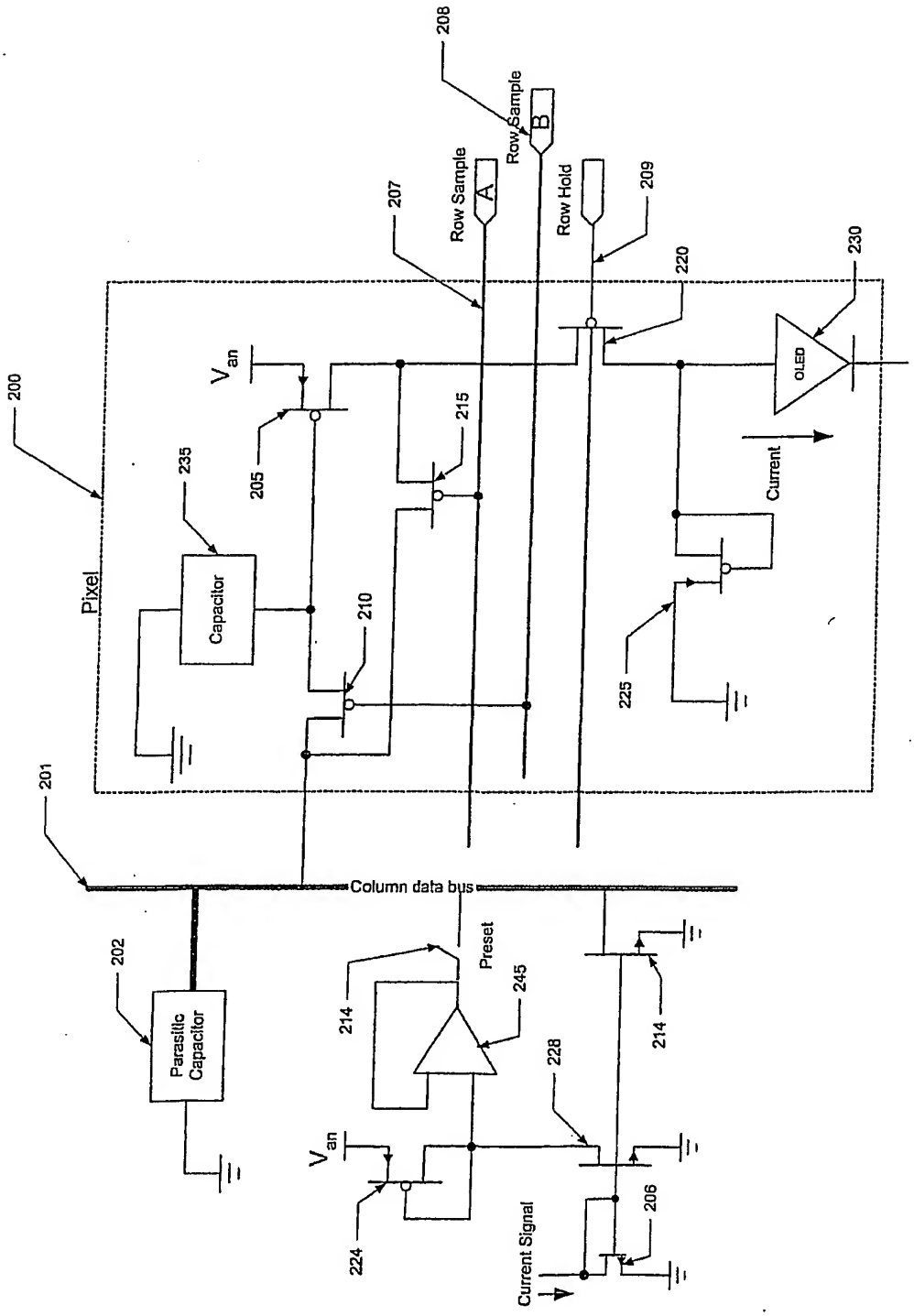
208
Row Sample
B
Row Sample
A
Row Hold
209
207
220
230
OLED
V_{an}
200
205
215
235
Current
Pixel
Capacitor
210
225
201
Column data bus
202
Parasitic Capacitor
Preset
214
245
214
228
V_{an}
224
206
Current Signal

Figure 5

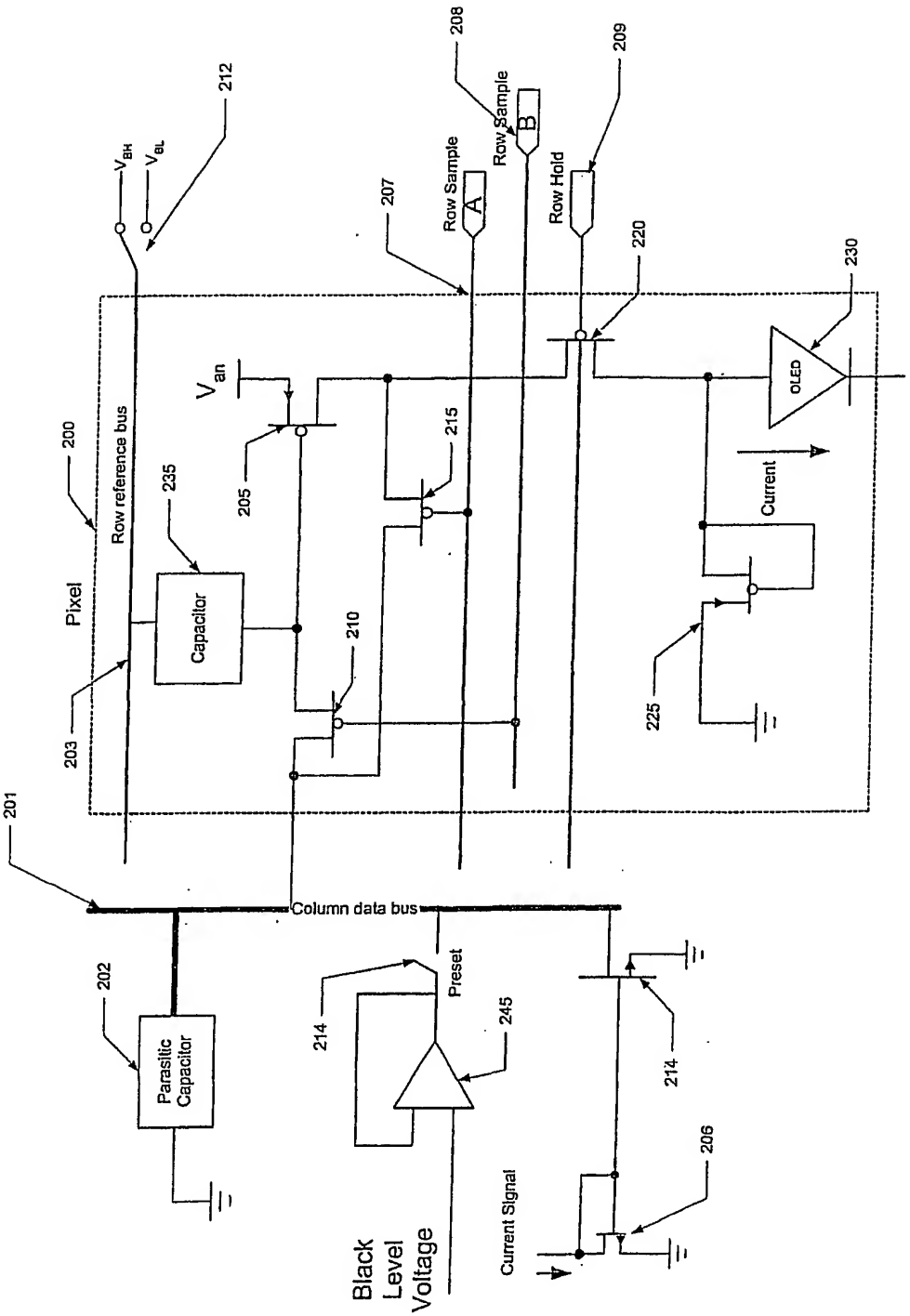
V_{BH}
V_{BL}
212
208
209
Row Sample
A
Row Sample
B
Row Hold
207
220
230
OLED
V_{an}
205
215
Current
200
Row reference bus
235
Pixel
Capacitor
210
203
225
201
Column data bus
202
Parasitic Capacitor
214
Preset
245
214
206
Black Level Voltage
Current Signal

Figure 6

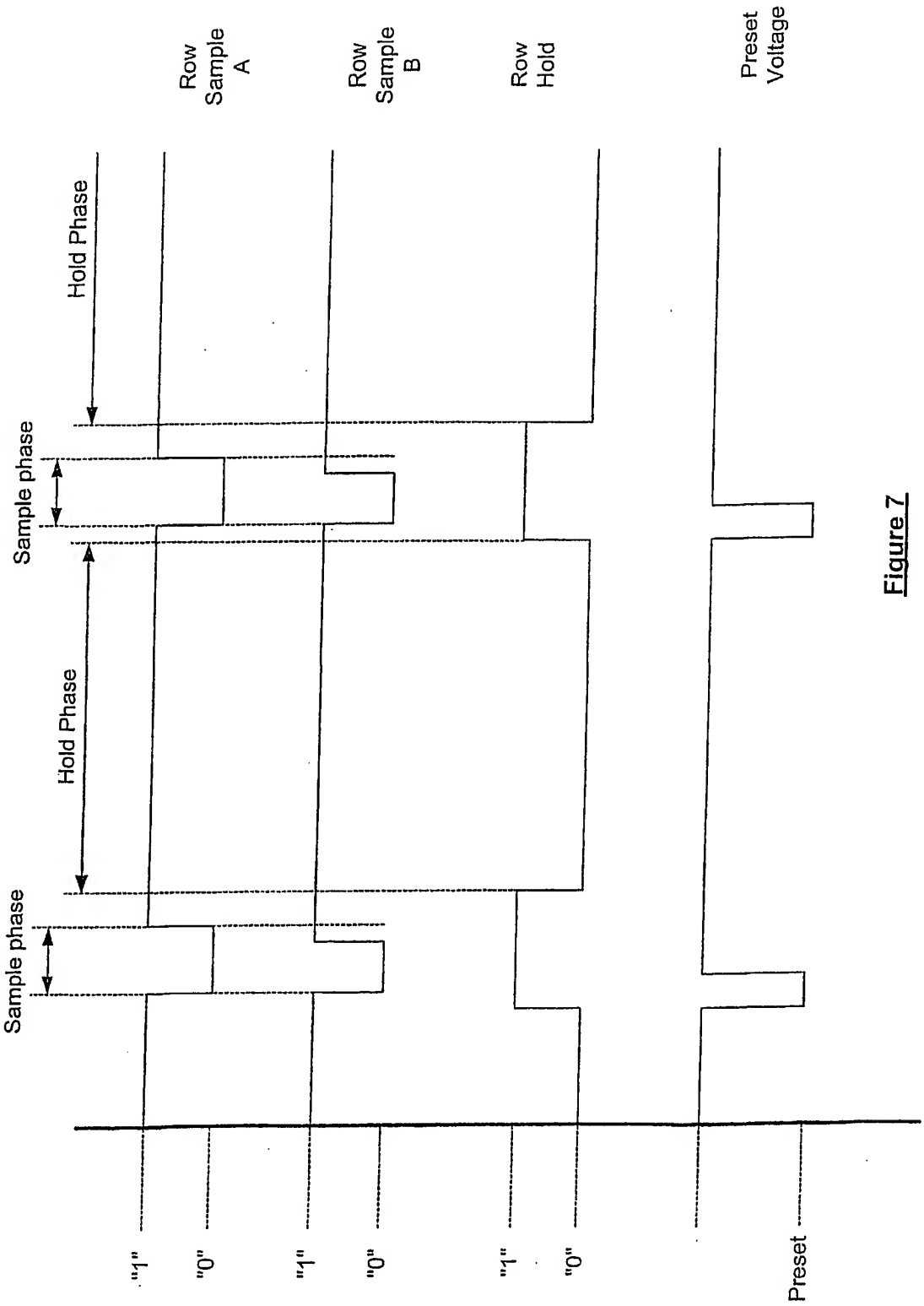
Row Sample A
Row Sample B
Row Hold
Preset Voltage
Hold Phase
Sample phase
Hold Phase
Sample phase
"1"
"0"
"1"
"0"
"1"
"0"
Preset

Figure 7

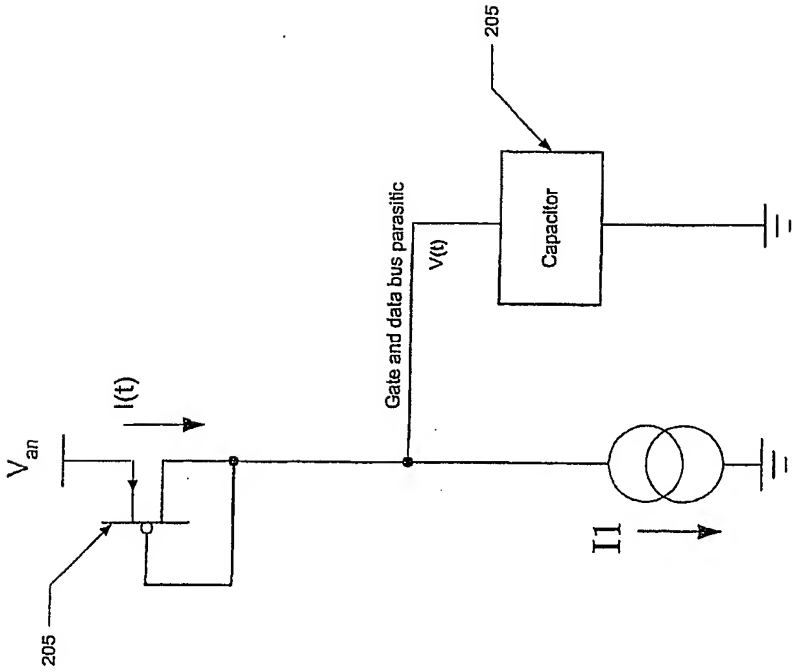

Figure 8

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(71) Applicant: eMagin Corporation [US/US]; 2070 Route 52, Hopewell Junction, NY 12533 (US).

(72) Inventors: PRACHE, Oliver, F.; 213 Manville Road, Pleasantville, NY 10570 (US). HONGJIN, Eric, Kim; 3 Preston Court, Bedford, MA 01730 (US). SASHI, D., Malaviya; 5 Orbit Lane, Hopewell Junction, NY 12533 (US). HAIQUNG, Lin; 6850 Sanctuary Court, Elkridge, MD 21075 (US). NAVAISKY, Eric; 844 Governors Run, Ellicott City, MD 21043 (US). EBNER, John; 1900 Thames Street #332, Baltimore, MD 21231 (US).

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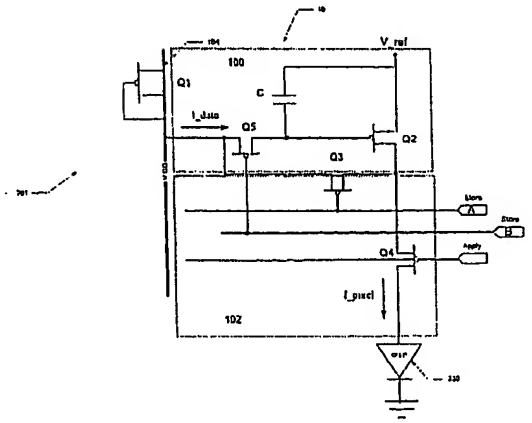
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A CURRENT-TYPE DRIVER FOR ORGANIC LIGHT EMITTING DIODE DISPLAYS



(57) Abstract: An OLED Driver circuit decreases capacitance charging time in the driver circuit by providing a high current signal to the circuit during a sample phase which rapidly charges the capacitances. A lower current signal is then provided during a hold phase to drive the corresponding OLED. The current levels are produced by operating the current driver of the circuit in the sub-threshold region where the output current is exponentially proportional to a reference voltage. The reference voltage may be controlled to provide a difference in reference voltage that produces the desired output current reduction. The driver circuit also includes a voltage driver that pre-charges the current driver gate to reduce settling time. The pre-charge level is provided during an initial portion of a sample phase to reduce the time it takes for the voltage at a current driver gate of the circuit to reach the desired signal level. The pre-set voltage is either selected by reference to the input signal level or by reference to a global level. In one implementation the global level is the black-level voltage for the corresponding display.

WO 02/071379 A3

INTERNATIONAL SEARCH REPORT

In ional Application No
PCT/US 01/22504

A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99 38148 A (FED CORP ;MALAVIYA SHASHI (US); HOWARD WEBSTER E (US); PRACHE OLIV) 29 July 1999 (1999-07-29) page 10, line 17 -page 15, line 9; figures 3,5-8	1-3,5, 11,12,14
X	WO 99 65011 A (KONINKL PHILIPS ELECTRONICS NV ;PHILIPS SVENSKA AB (SE)) 16 December 1999 (1999-12-16)	1-3,5
A	page 12, line 31 -page 13, line 27; figures 2-4 page 14, line 26-31 page 15, line 15-17	7-10,13
	-/--	

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Date of the actual completion of the international search	Date of mailing of the international search report
7 February 2003	21/02/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Amian, D

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

nformation on patent family members

In ɔnal Application No
PCT/US 01/22504

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